STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

1. to 11. **(Cancelled)**

12. **(Previously presented)** A method of dividing a power source voltage comprising the steps of:

providing a voltage divider circuit having a first transistor including a first transistor gate electrode having a first transistor gate electrode area and a second transistor including a second transistor gate electrode having a second transistor gate electrode area;

applying the power source voltage to said voltage divider circuit; and

dividing the power source voltage according to the ratio of said first transistor gate electrode area to said second transistor gate electrode area, wherein said ratio is calculated using the following non-linear function solved by numerical iteration

$[6.1434 \times \text{Log}(V2)] + [2.6286 \times \{\text{Log}(V2)\}^2] + [1.3483 \times \{\text{Log}(V2)\}^3] + [0.37073 \times \{\text{Log}(V2)\}^4] + [0.036284 \times \{\text{Log}(V2)\}^5] + \{\text{Log } R\} - [6.1434 \times \text{Log}(V1)] - [2.6286 \times \{\text{Log}(V1)\}^2] - [1.3483 \times \{\text{Log}(V1)\}^3] - [0.37073 \times \{\text{Log}(V1)\}^4] - [0.036284 \times \{\text{Log}(V1)\}^5] = 0$, where

V1 = desired voltage across said first transistor = VDD x VR/(VR + 1)
V2 = desired voltage across said second transistor = VDD/(VR + 1)
VR = V1/V2
VDD = applied power source voltage
R = said ratio of said second transistor gate electrode area to said first transistor gate electrode area.

13. to 19. **(Cancelled)**

20. **(Previously presented)** A method of designing a circuit for dividing voltage, comprising the steps of:

providing a first transistor including a gate electrode having an area, a source, and a drain; and

providing a second transistor including a gate electrode having an area, a source, and a drain;

selecting said first transistor gate electrode area and said second transistor gate electrode area according to a predetermined ratio between the areas to provide a desired voltage division, wherein said ratio is calculated using the following non-linear function solved by numerical iteration

$[6.1434 \times \text{Log}(V2)] + [2.6286 \times \{\text{Log}(V2)\}^2] + [1.3483 \times \{\text{Log}(V2)\}^3] + [0.37073 \times \{\text{Log}(V2)\}^4] + [0.036284 \times \{\text{Log}(V2)\}^5] + \{\text{Log } R\} - [6.1434 \times \text{Log}(V1)] - [2.6286 \times \{\text{Log}(V1)\}^2] - [1.3483 \times \{\text{Log}(V1)\}^3] - [0.37073 \times \{\text{Log}(V1)\}^4] - [0.036284 \times \{\text{Log}(V1)\}^5] = 0$, where

V1 = desired voltage across said first transistor = VDD x VR/(VR + 1)
V2 = desired voltage across said second transistor = VDD/(VR + 1)
VR = V1/V2
VDD = applied power source voltage
R = said ratio of said second transistor gate electrode area to said first transistor gate electrode area

; and

joining said second transistor gate electrode with said first transistor source and said first transistor drain.

21. **(Cancelled)**

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